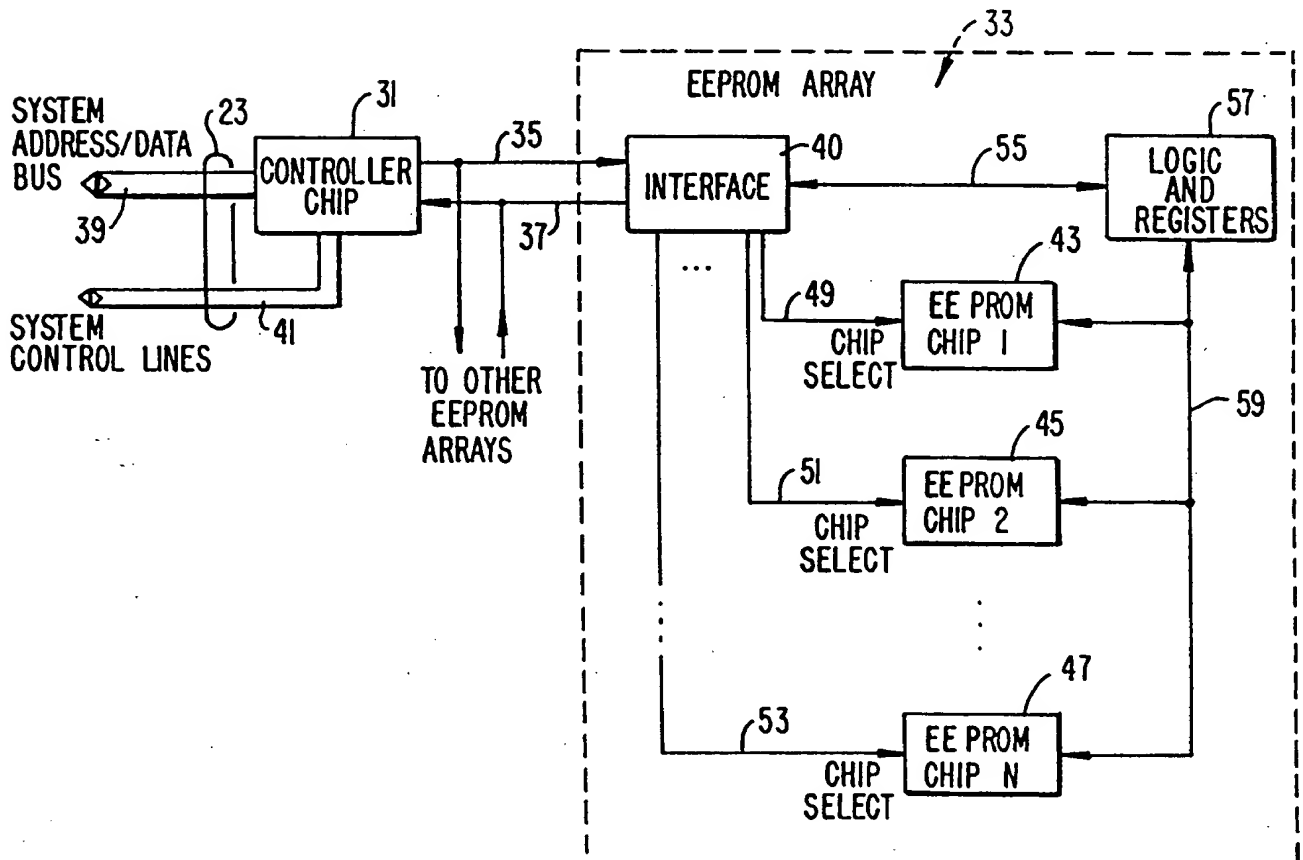
**FIG. 1A****FIG. 1B**

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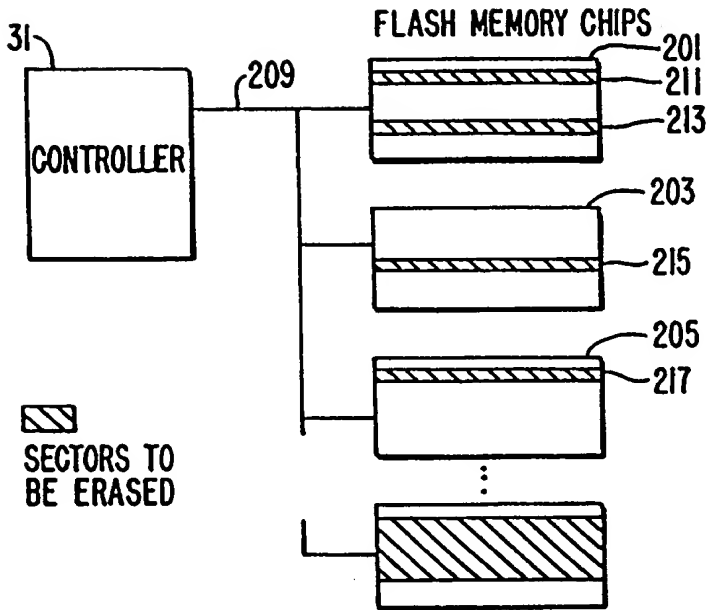


FIG. 2

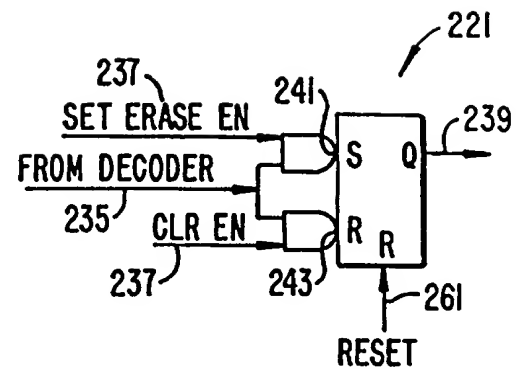


FIG. 3B

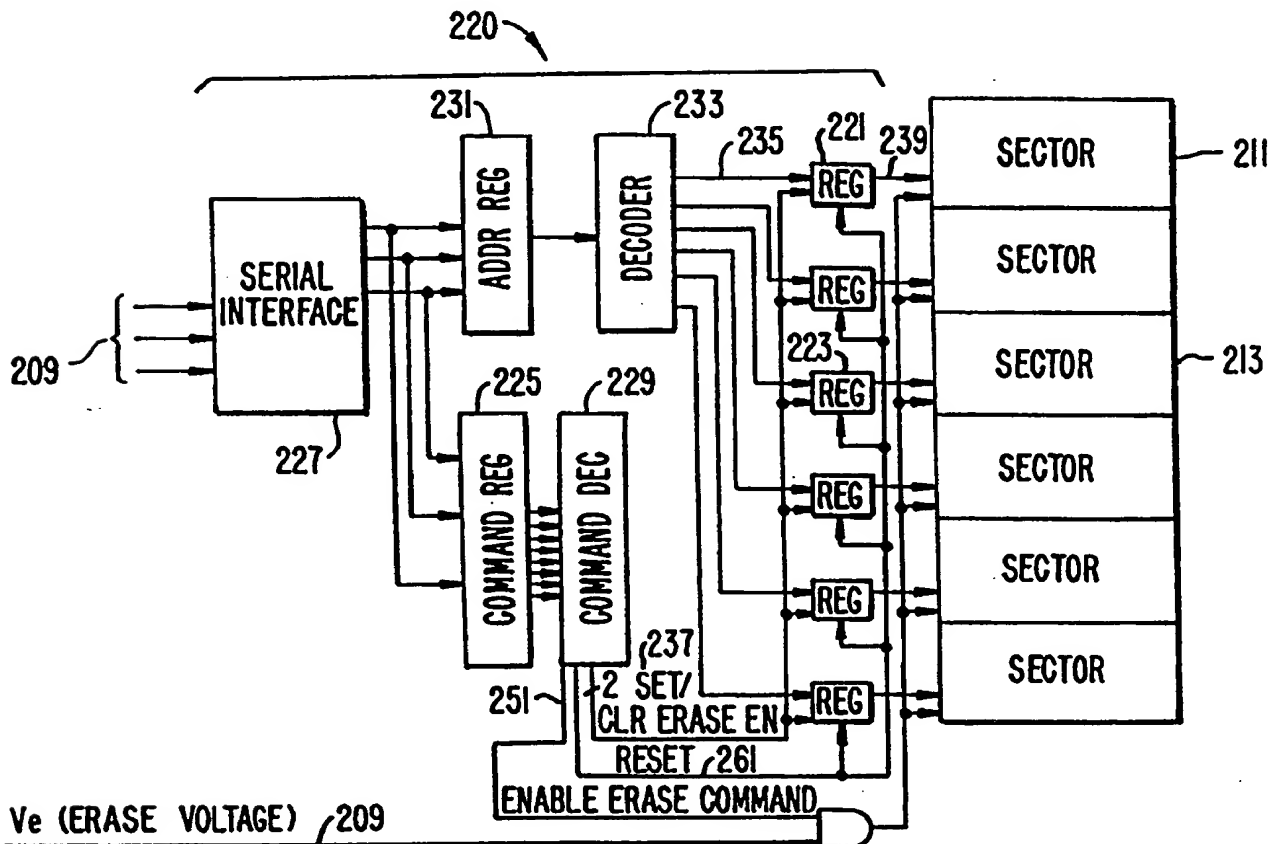


FIG. 3A

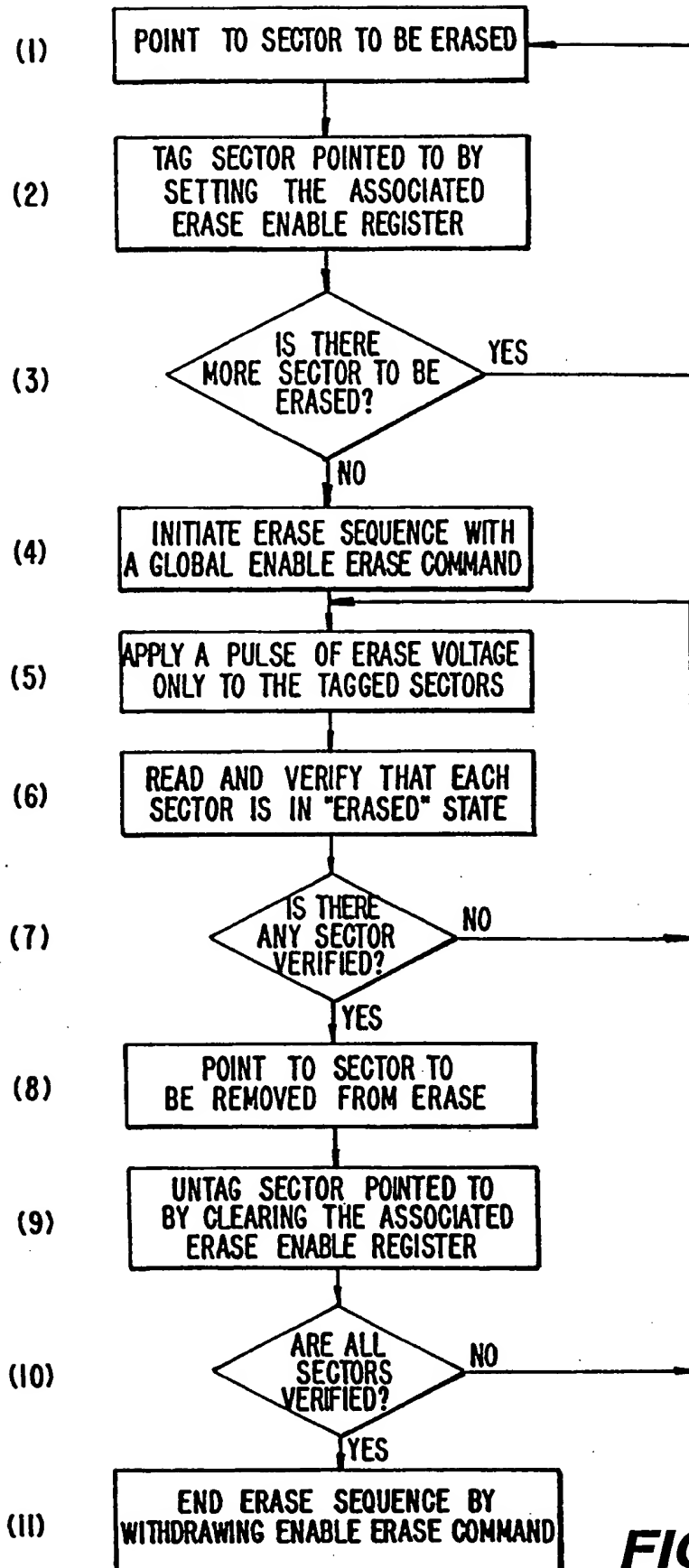
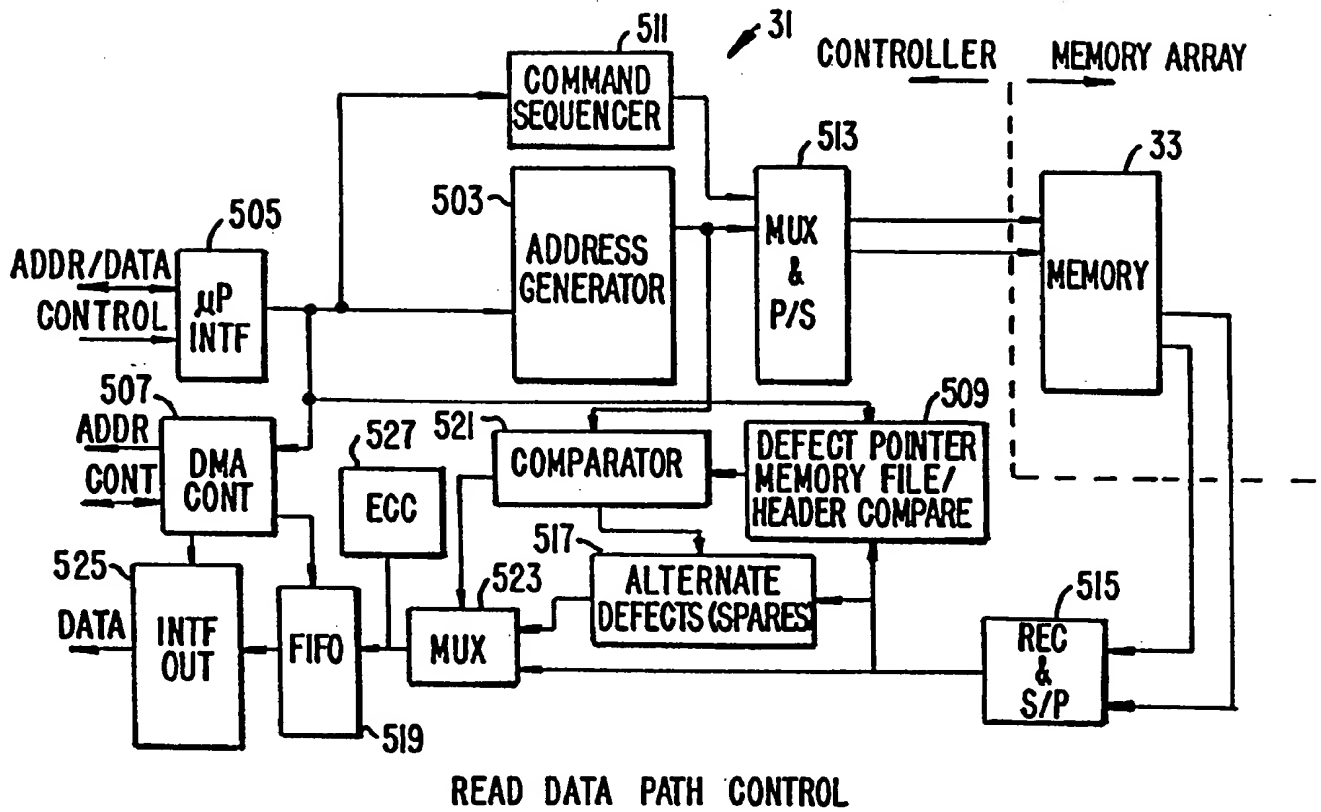
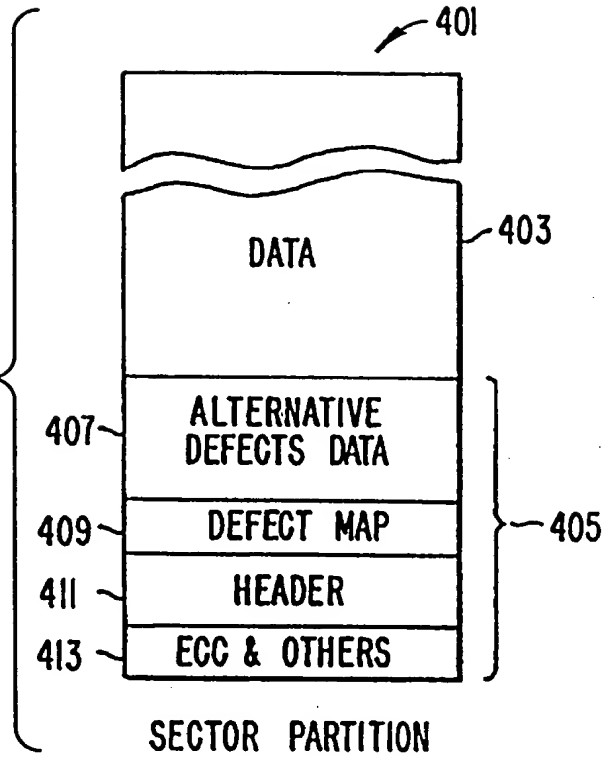


FIG. 4

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**FIG. 5**



**FIG. 6**

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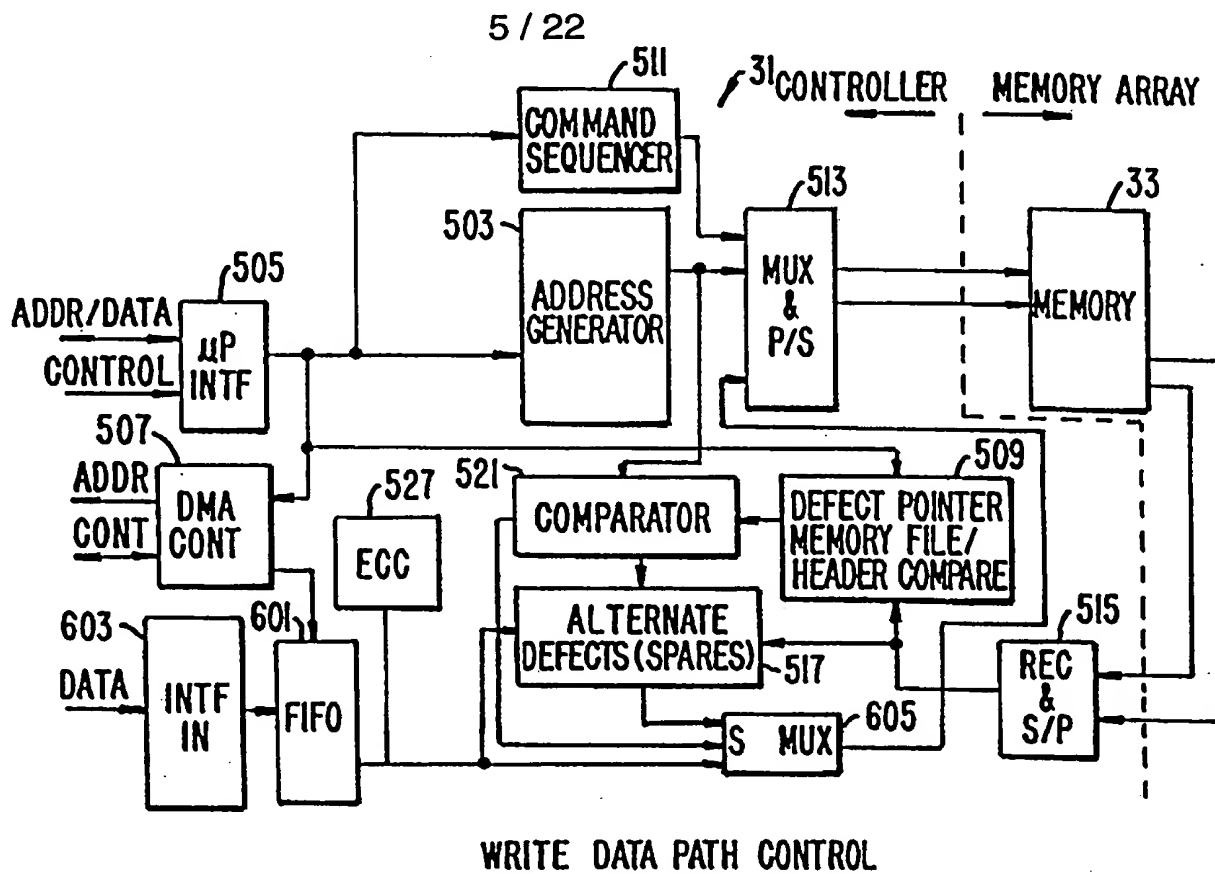


FIG. 7

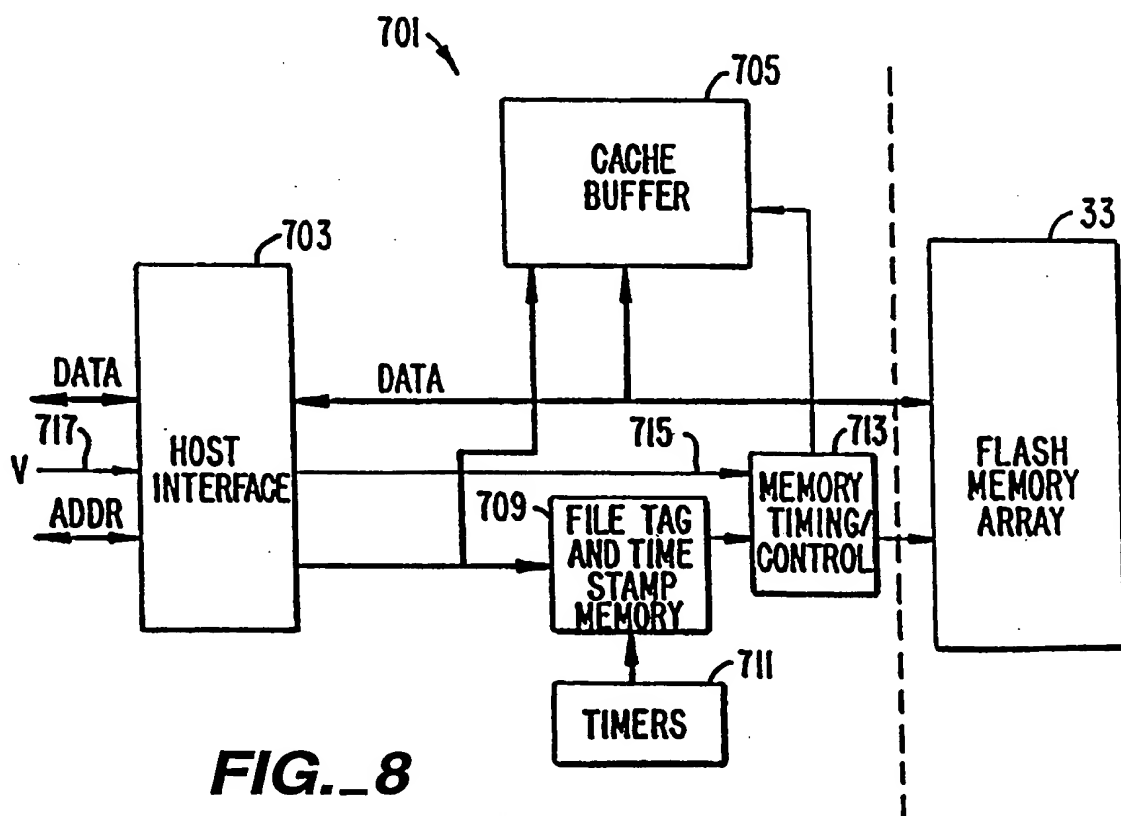
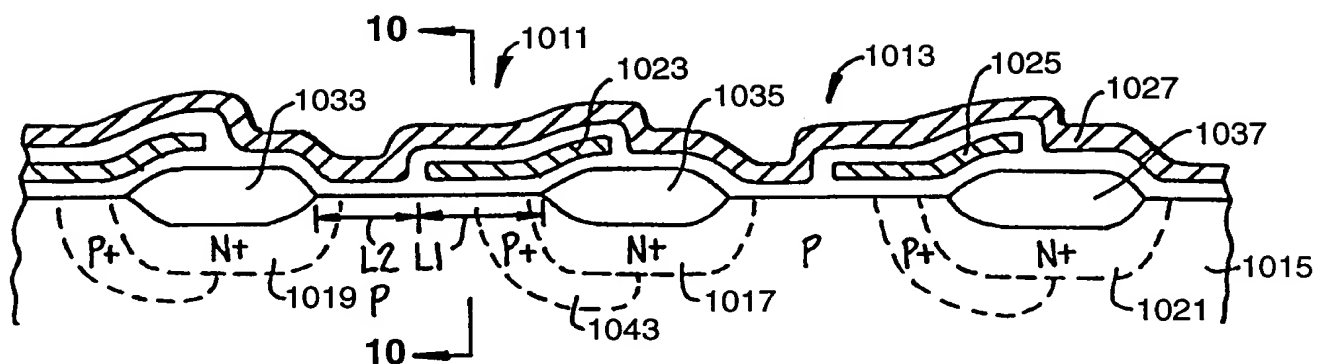
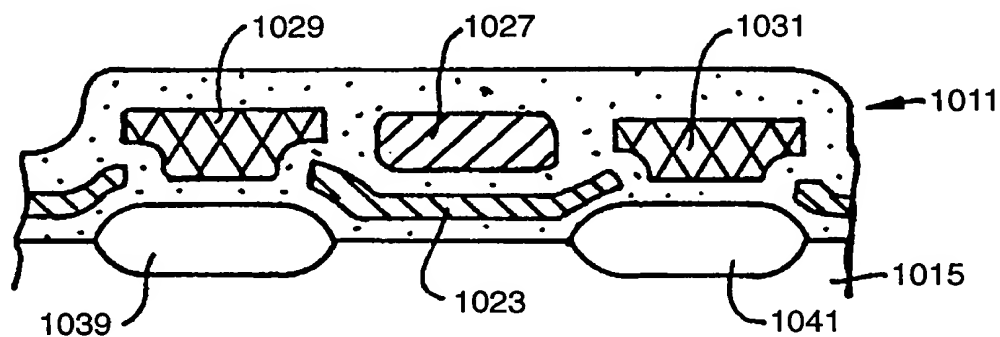


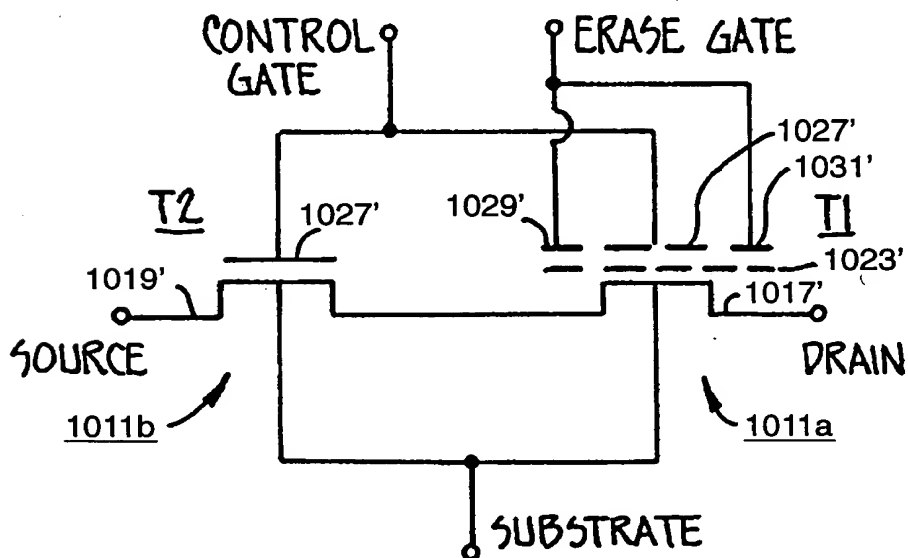
FIG. 8



**FIG. 9**



**FIG.\_10**



**FIG. 11**

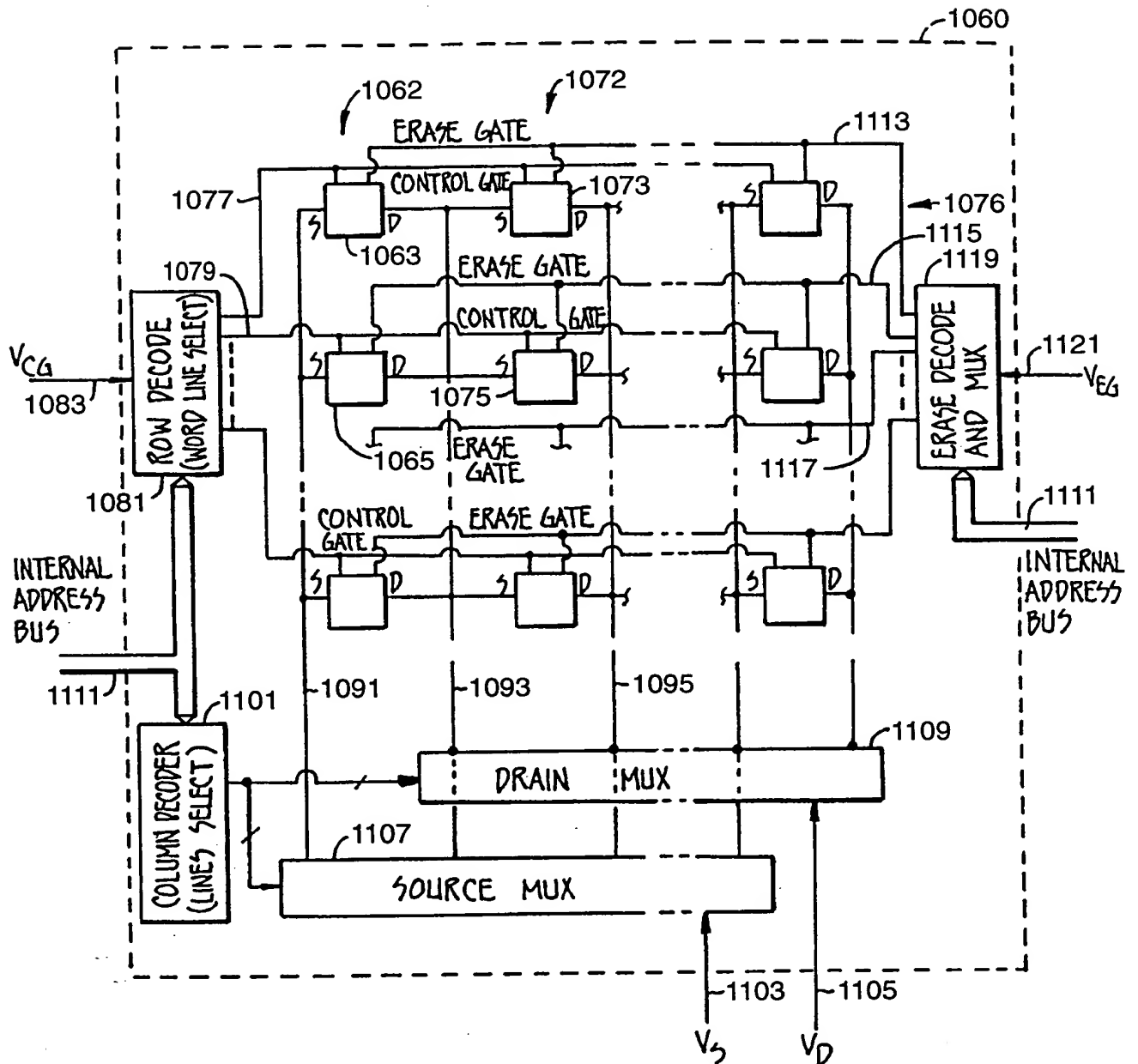


FIG. 12

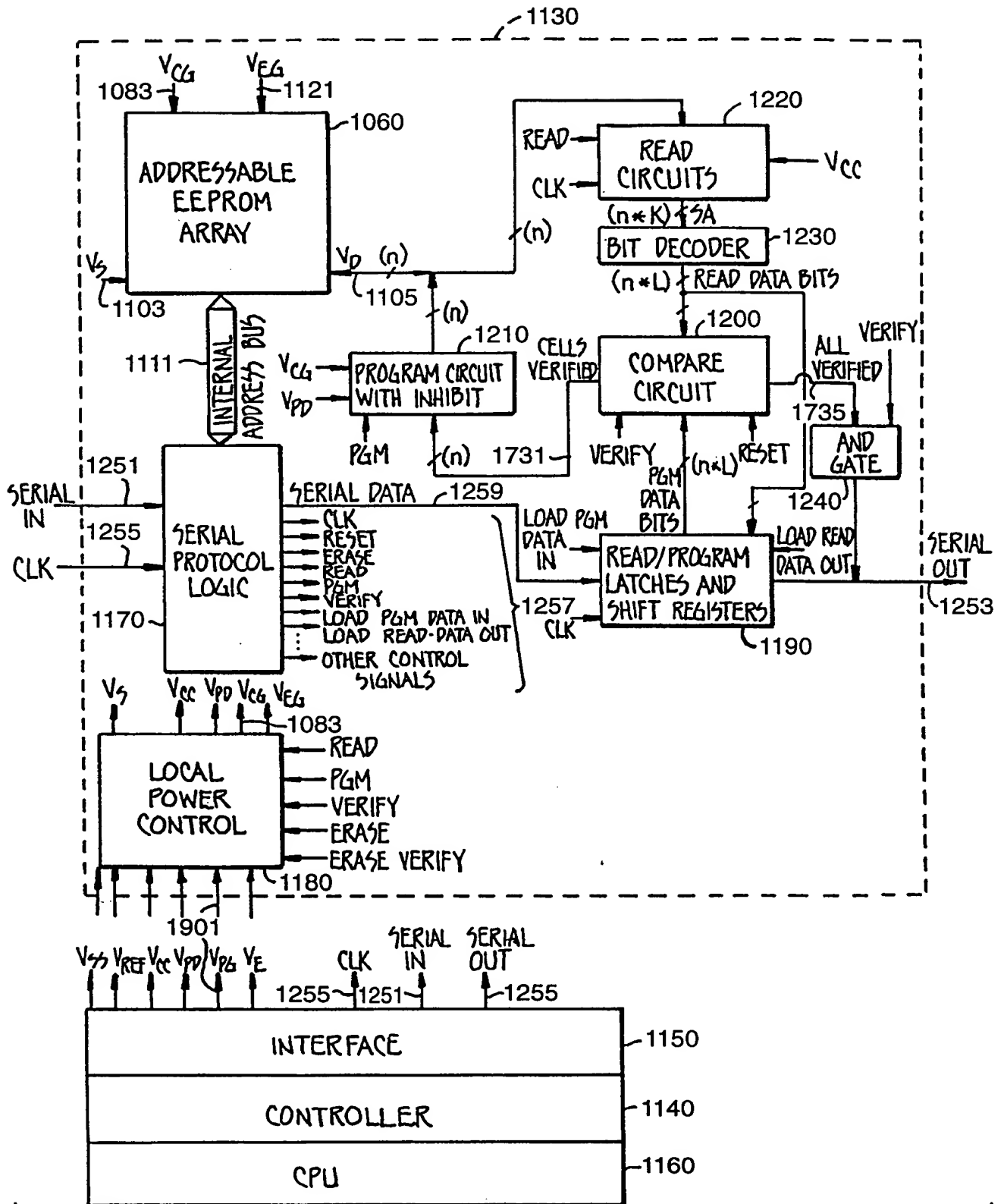


FIG. 13

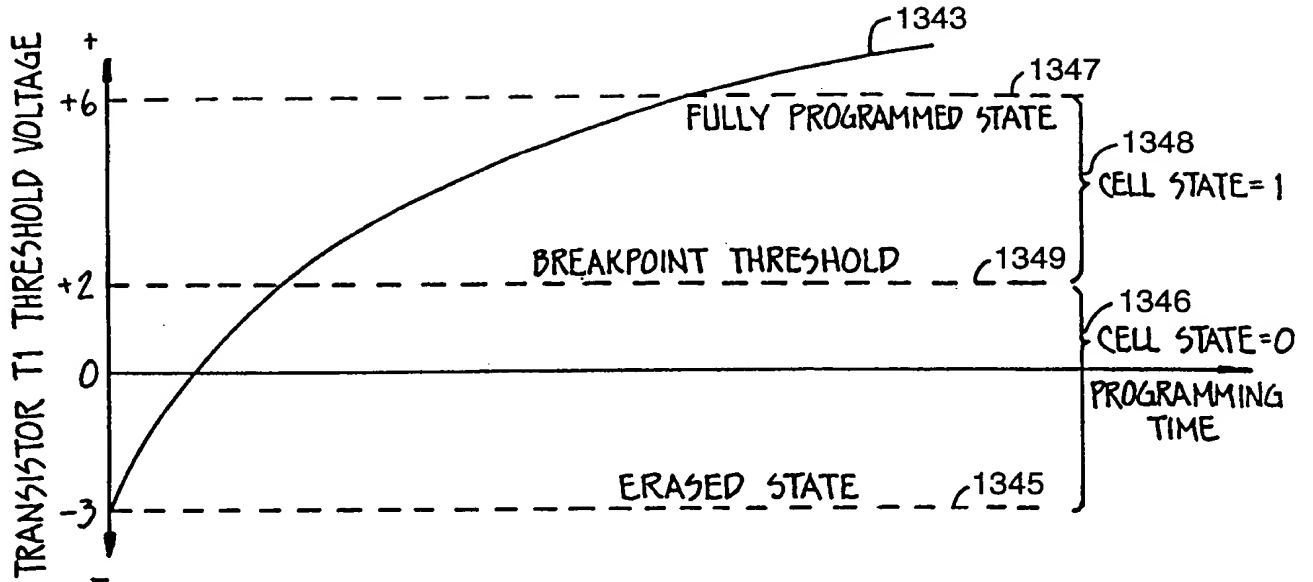


FIG. 14

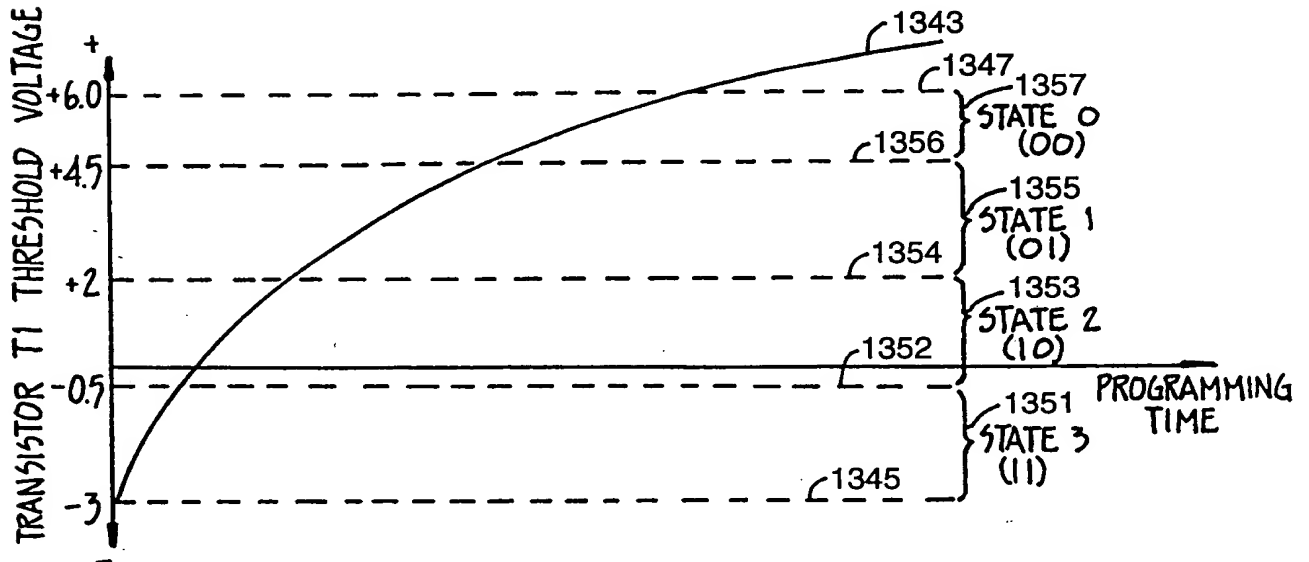


FIG. 15A

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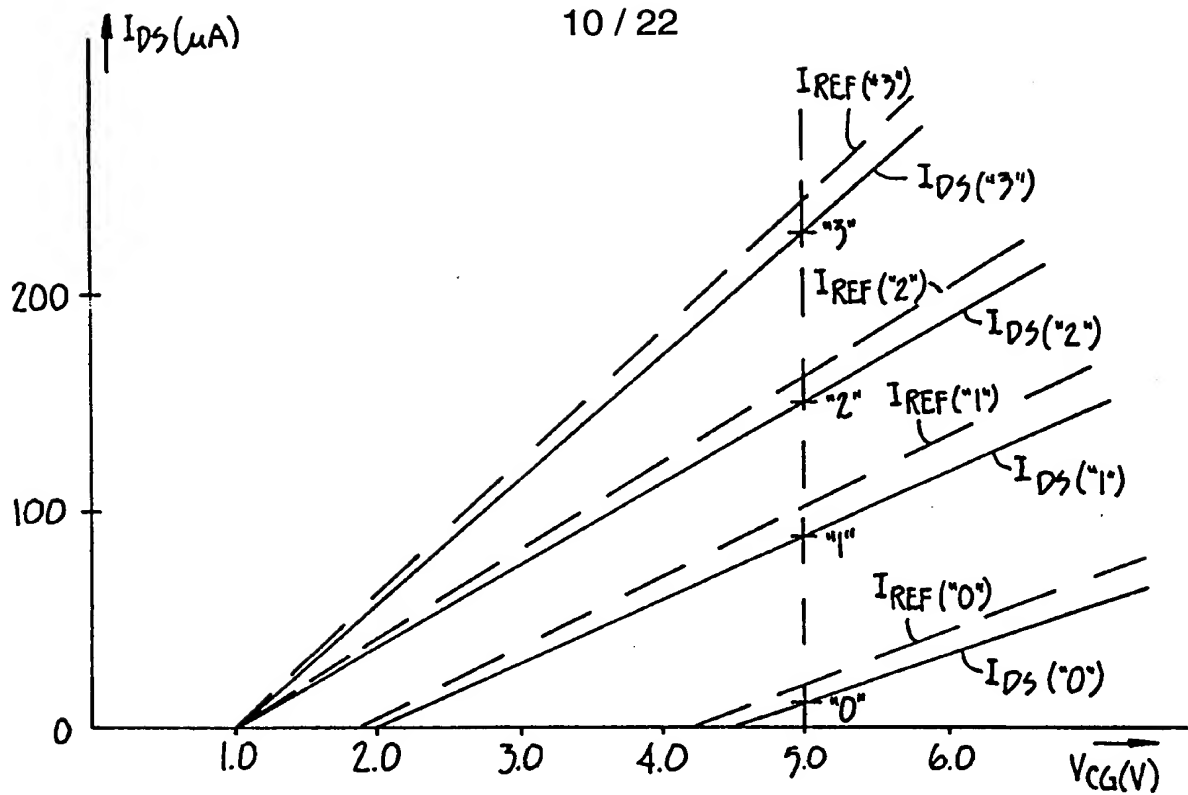


FIG.\_15B

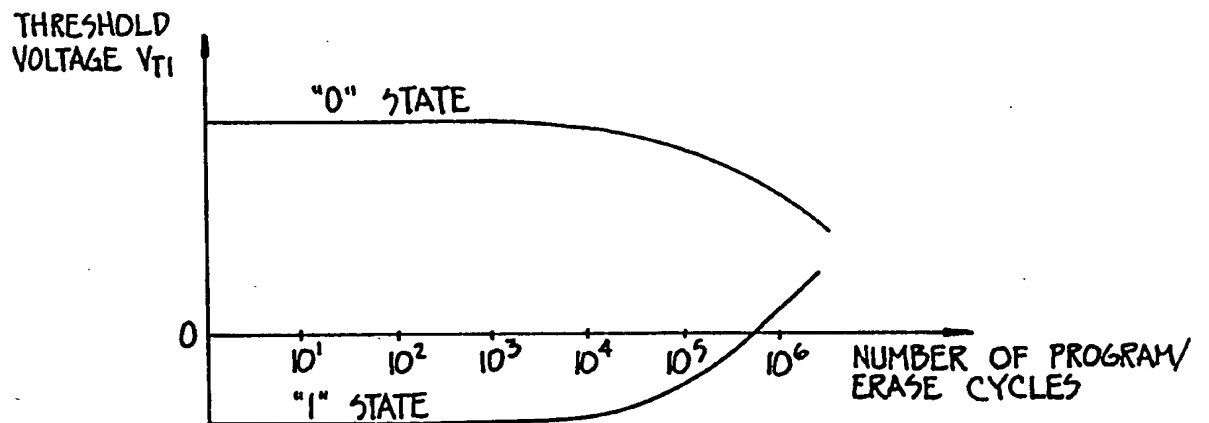


FIG.\_16A

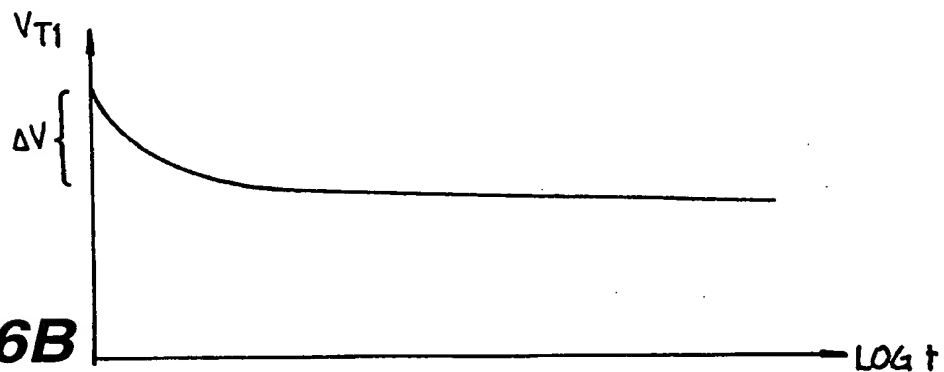


FIG.\_16B

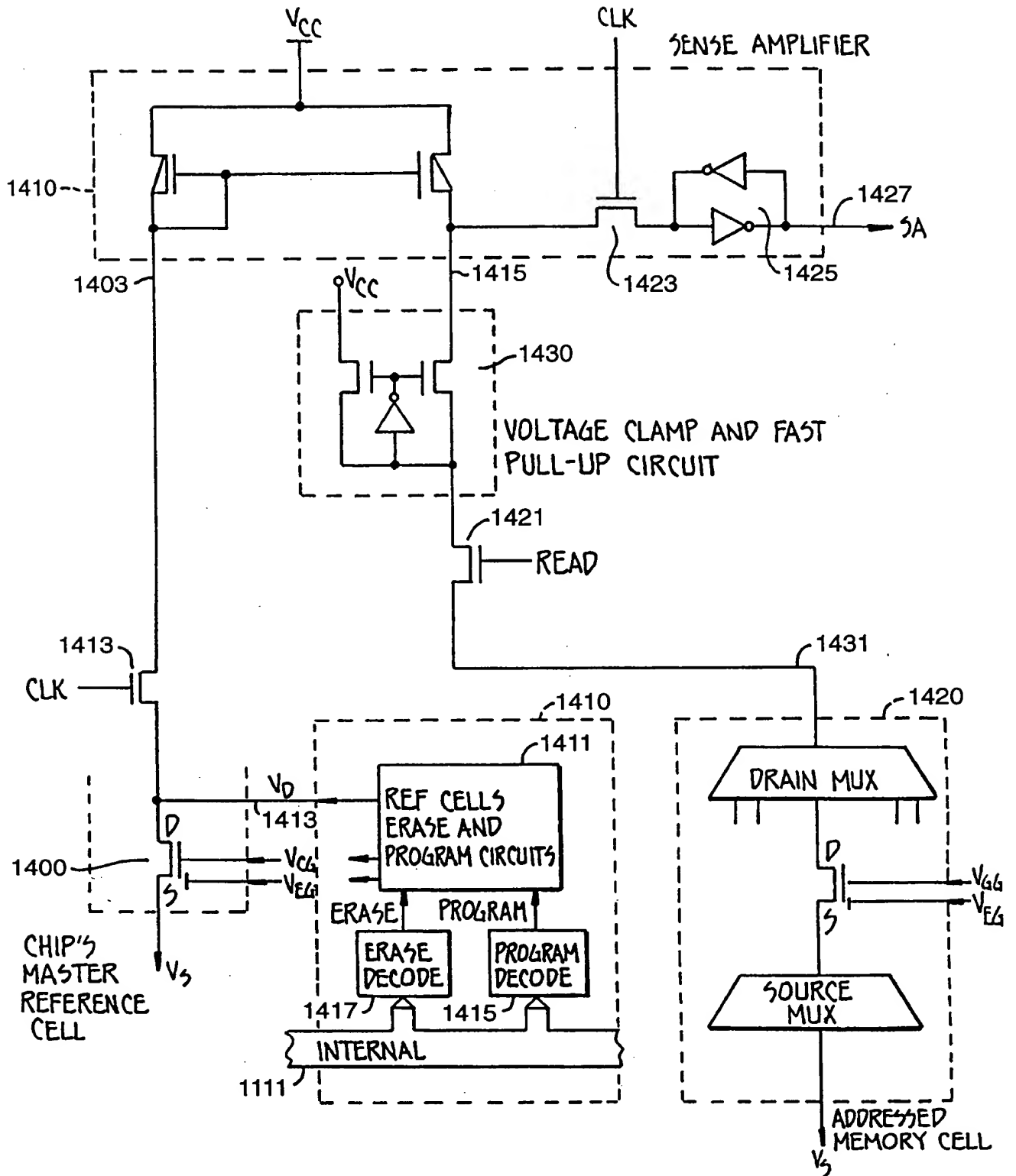
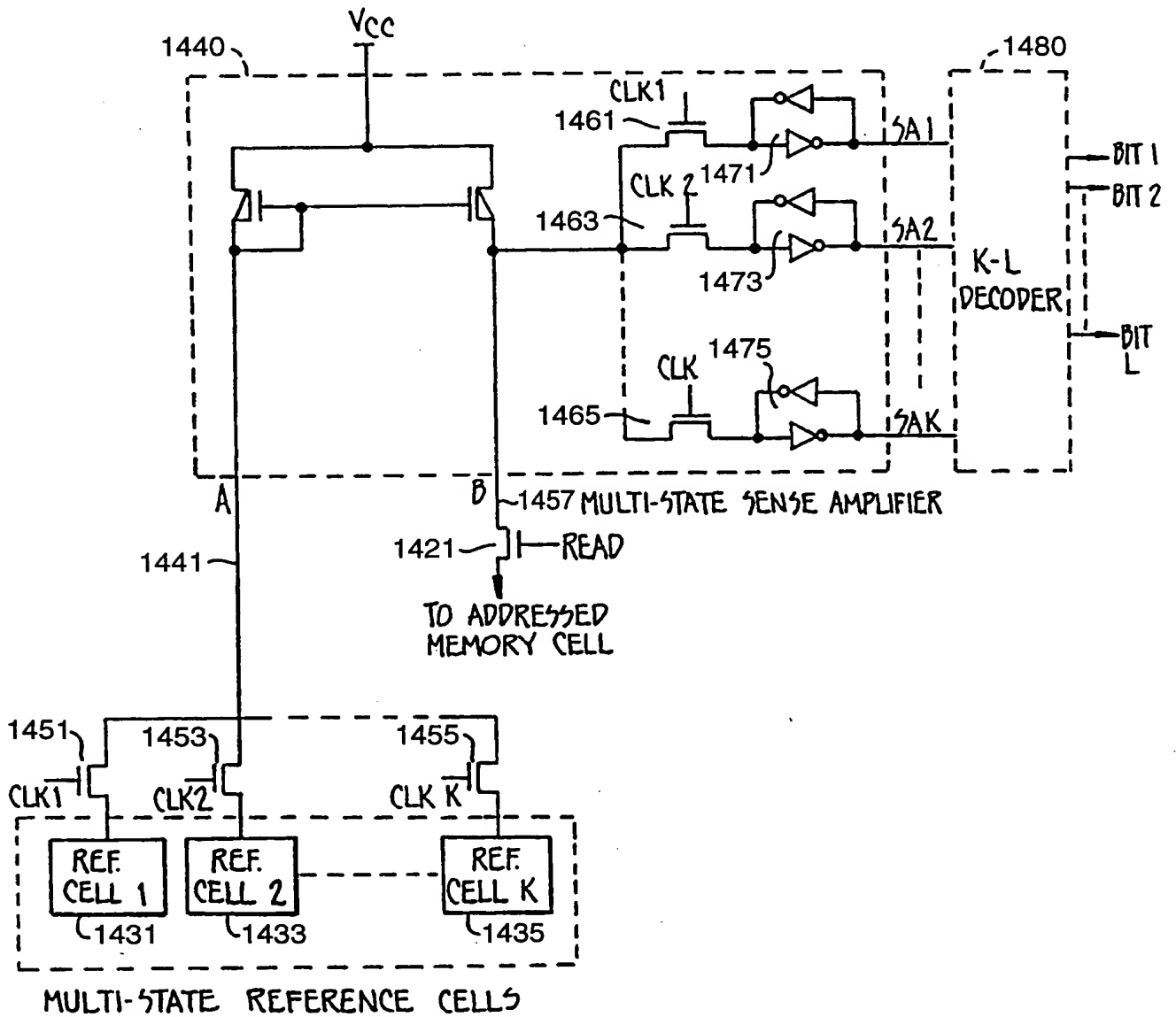
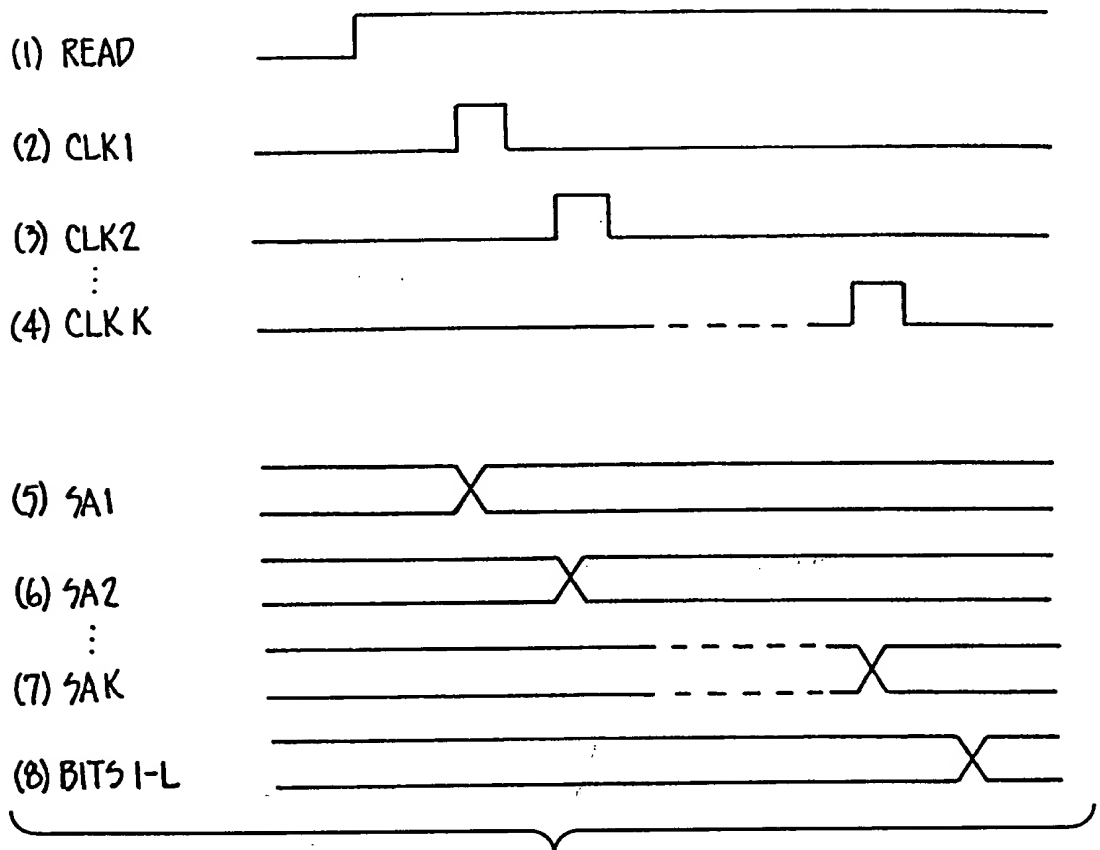
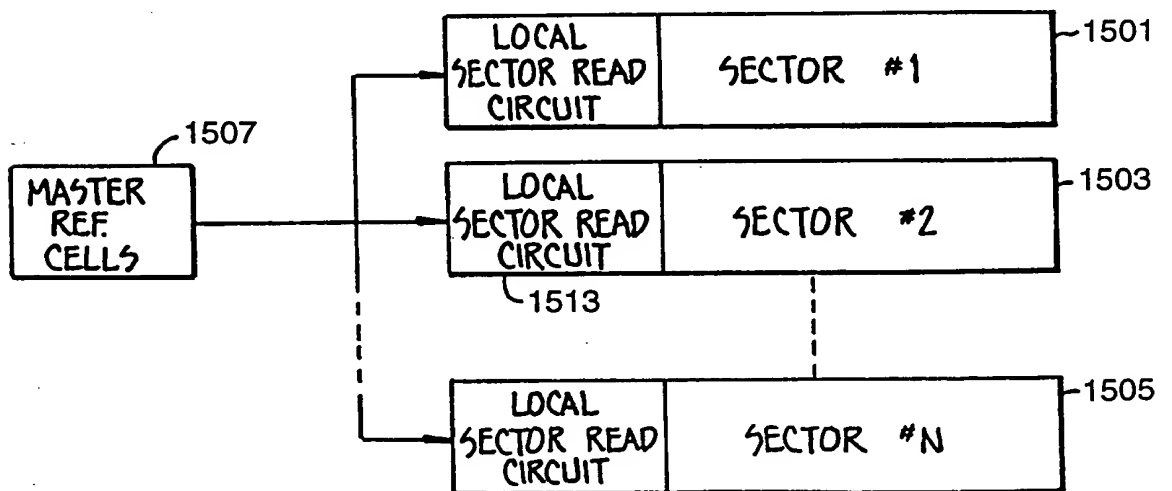


FIG. 17A

**FIG. 17B**

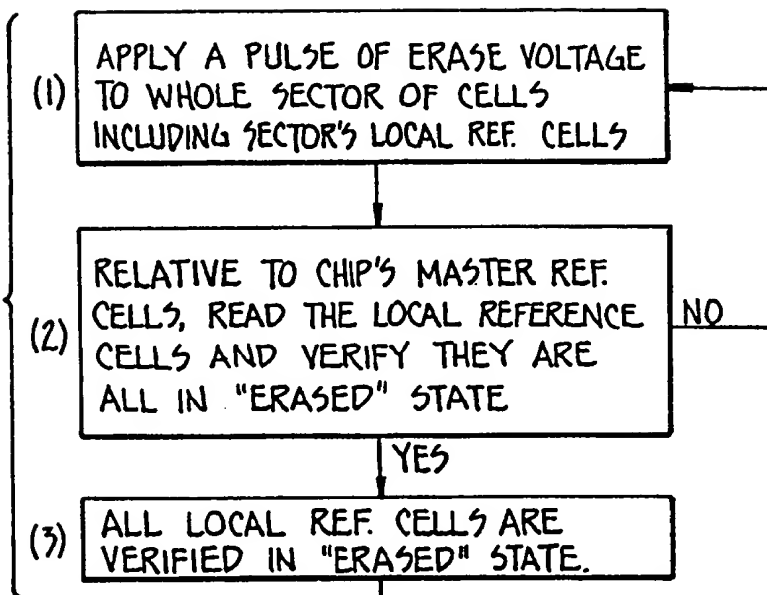


**FIG.\_17C**

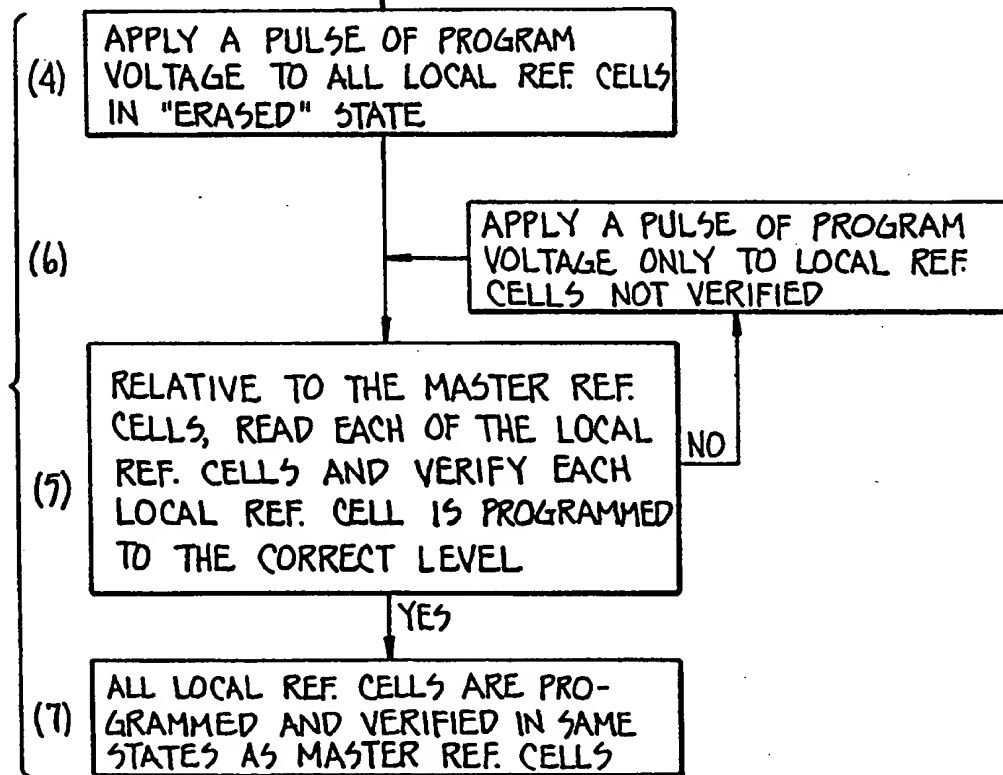


**FIG.\_18**

SECTOR LOCAL  
REF. CELLS ERASE  
AND VERIFY  
ALGORITHM

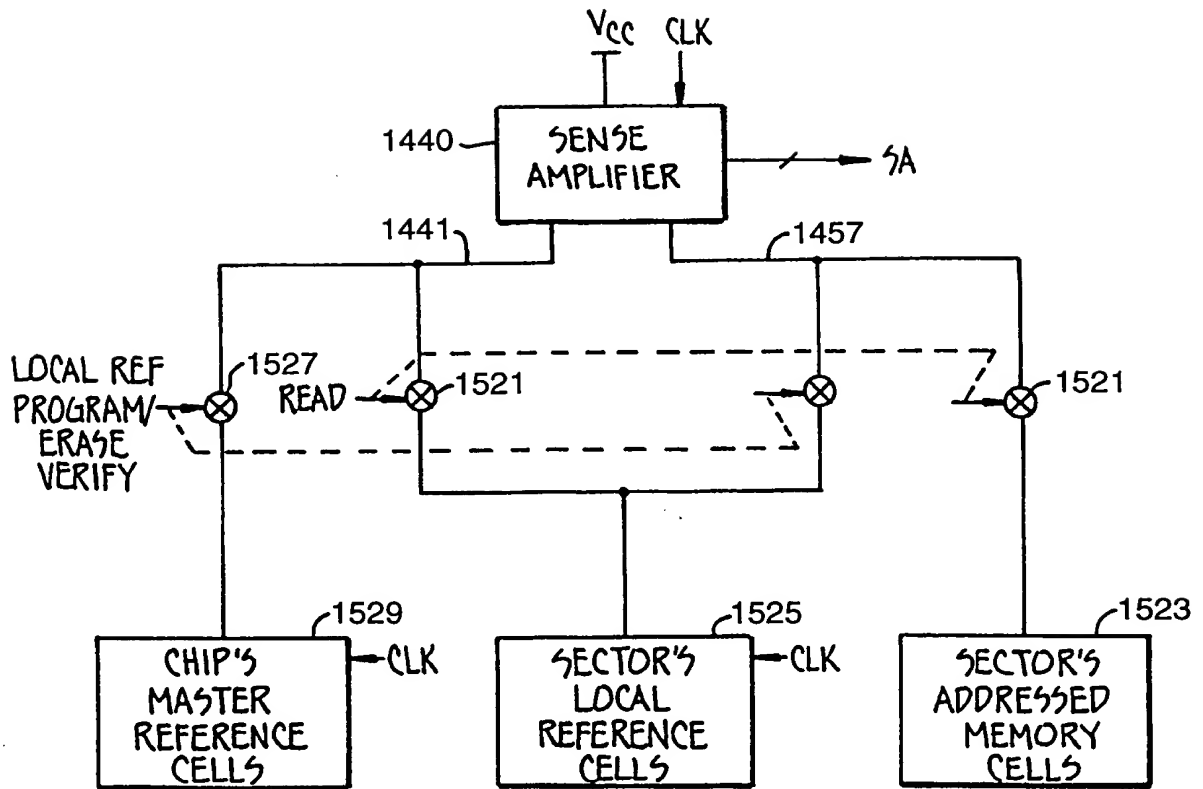


SECTOR'S LOCAL  
REF. CELLS  
PROGRAM AND  
VERIFY ALGORITHM

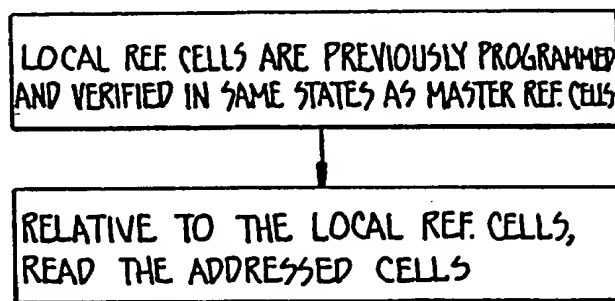


**FIG. 19**

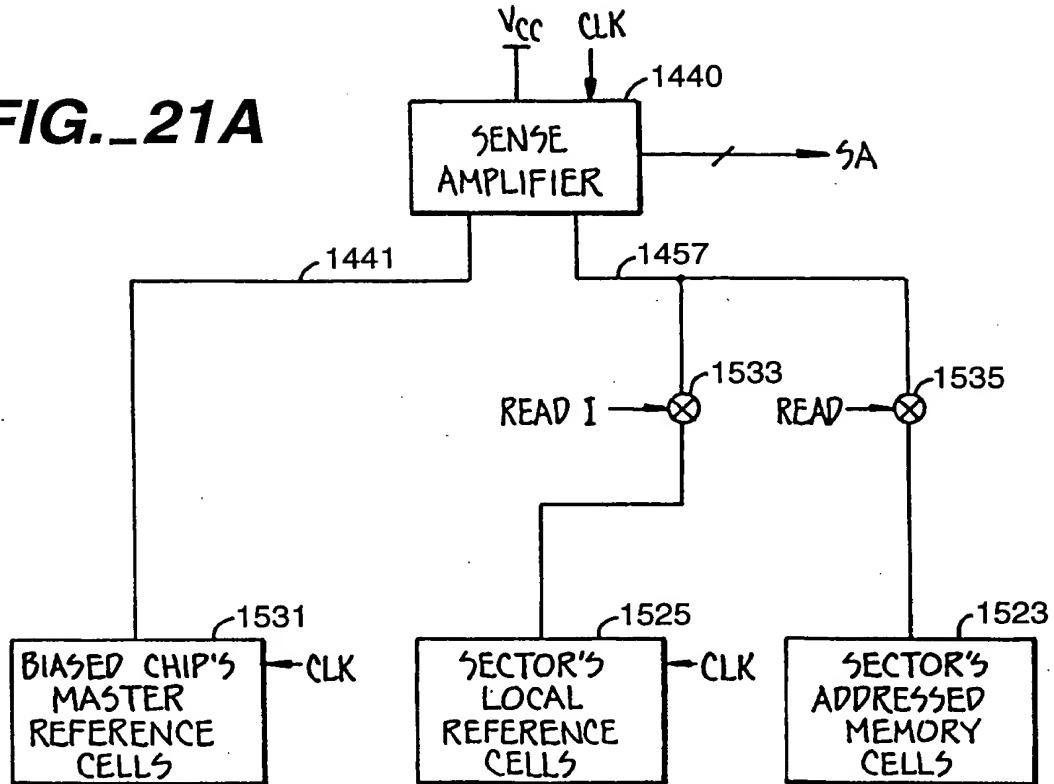
09188417 110998



**FIG.\_20A**

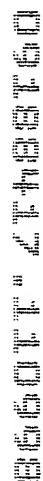


**FIG.\_20B**

**FIG.\_21A**

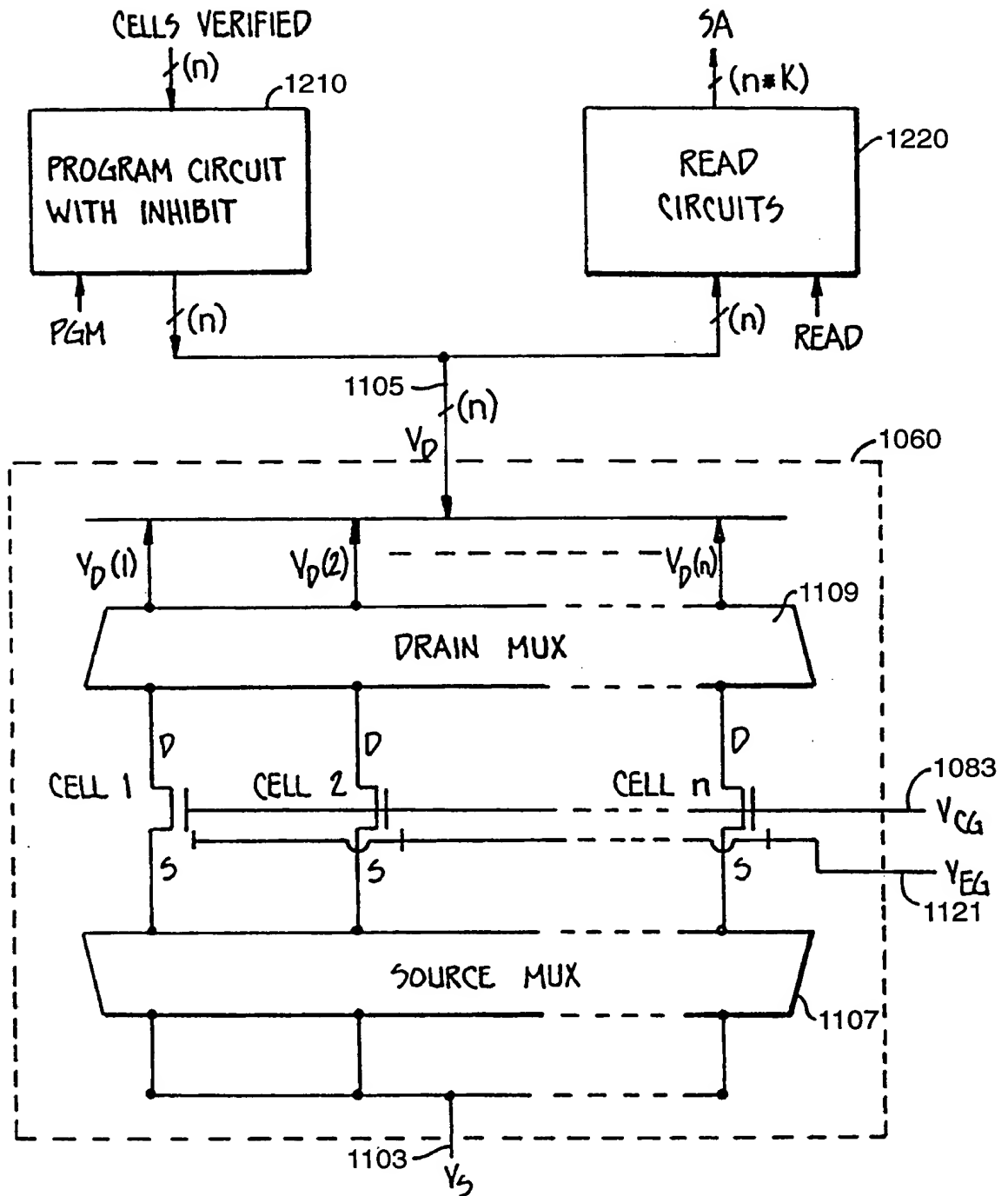
- (1) LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS
- (2) RELATIVE TO THE LOCAL REFERENCE CELLS READ THE MASTER REF. CELLS
- (3) DETERMINE THE DIFFERENCES, IF ANY AND BIAS. THE MASTER REF CELLS' CURRENTS SUCH THAT THE SAME READING IS OBTAINED RELATIVE TO THE BIASED MASTER REF. CELLS AS RELATIVE TO THE LOCAL REF. CELLS
- (4) RELATIVE TO THE BIASED MASTER REF. CELLS, READ THE ADDRESSED CELLS

**FIG.\_21D**



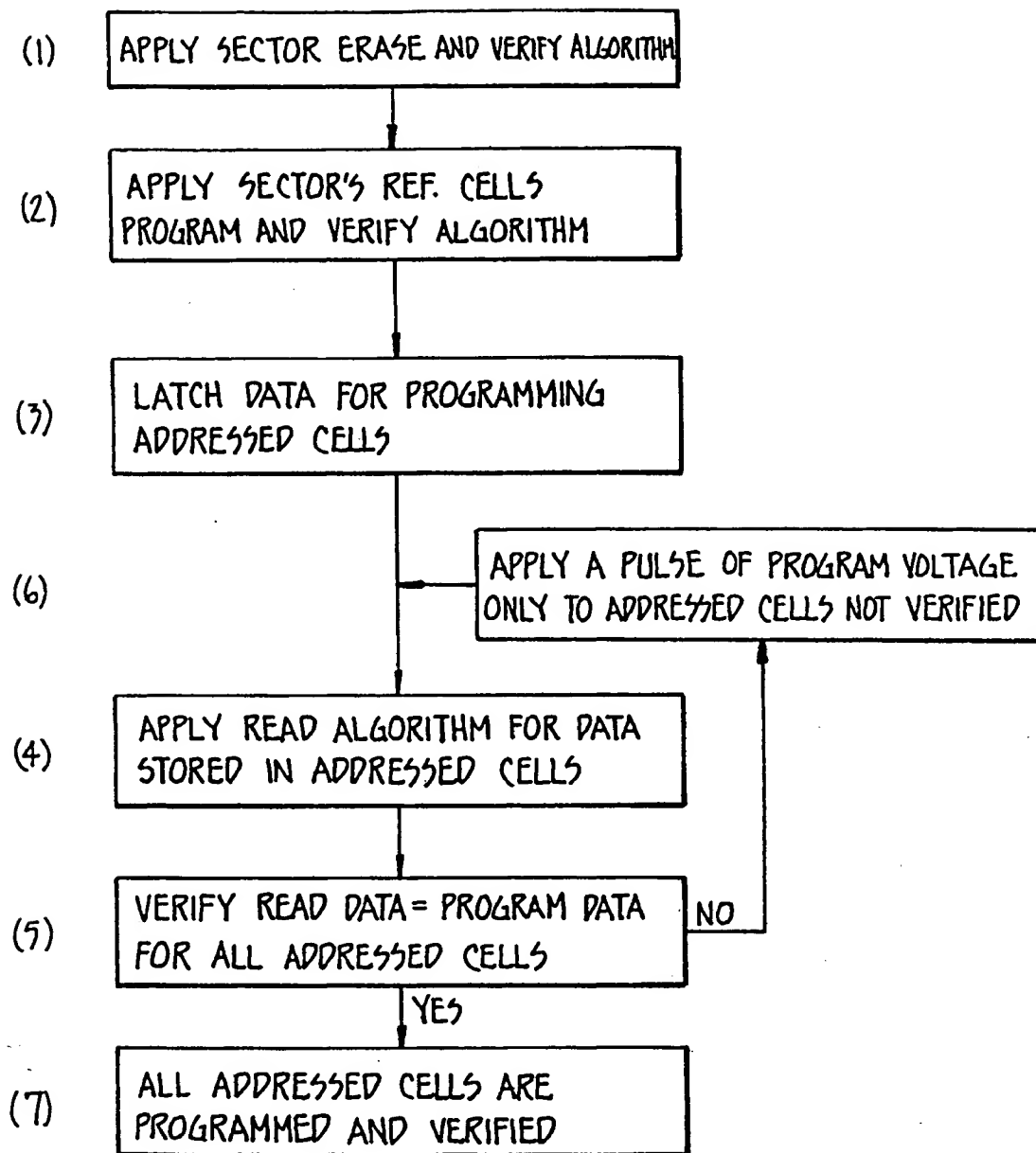
**FIG.\_21C**





READ/PROGRAM DATA PATHS FOR  $n$  CELLS IN PARALLEL

**FIG. 22**



PROGRAM ALGORITHM

**FIG. 23**

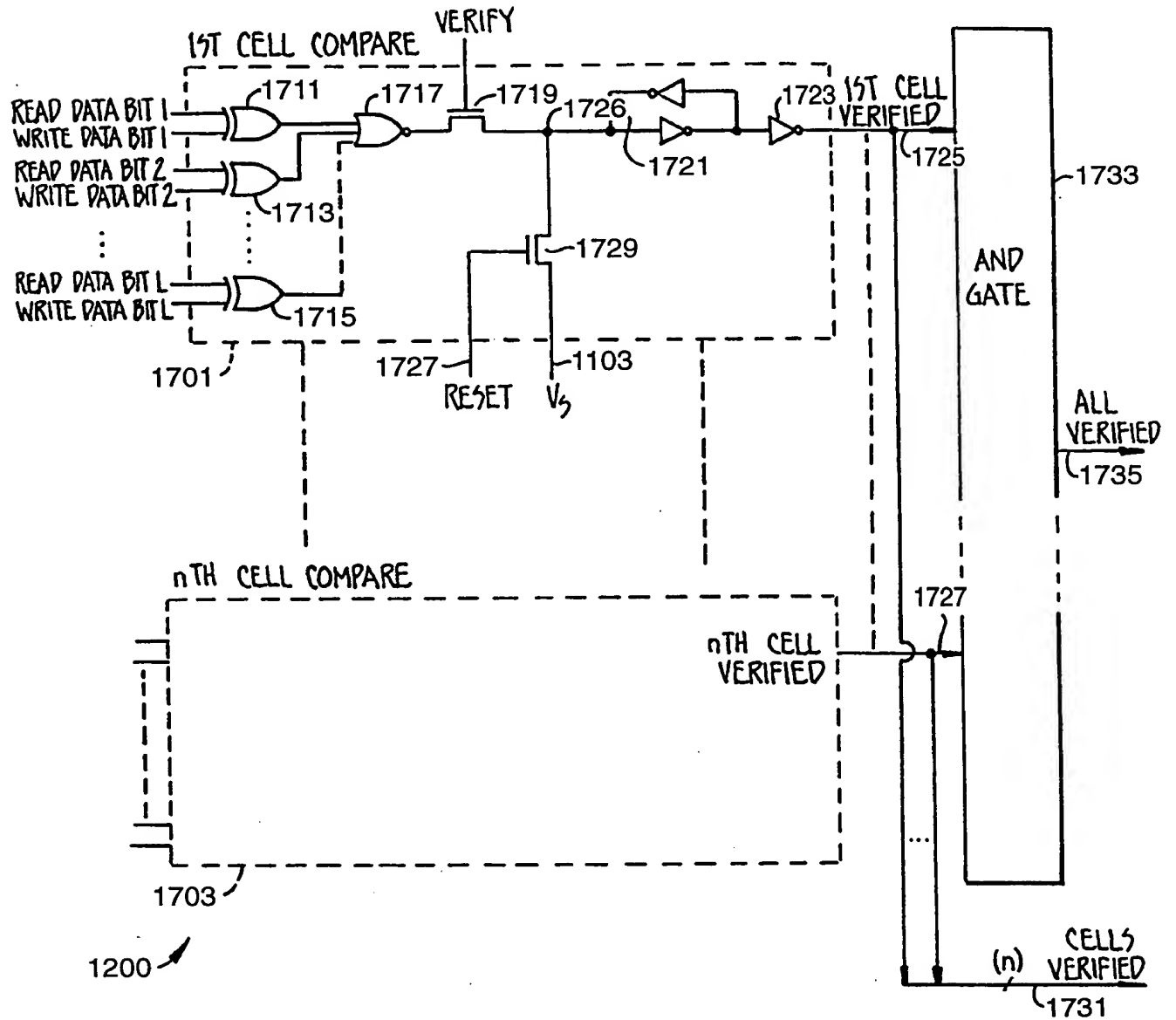
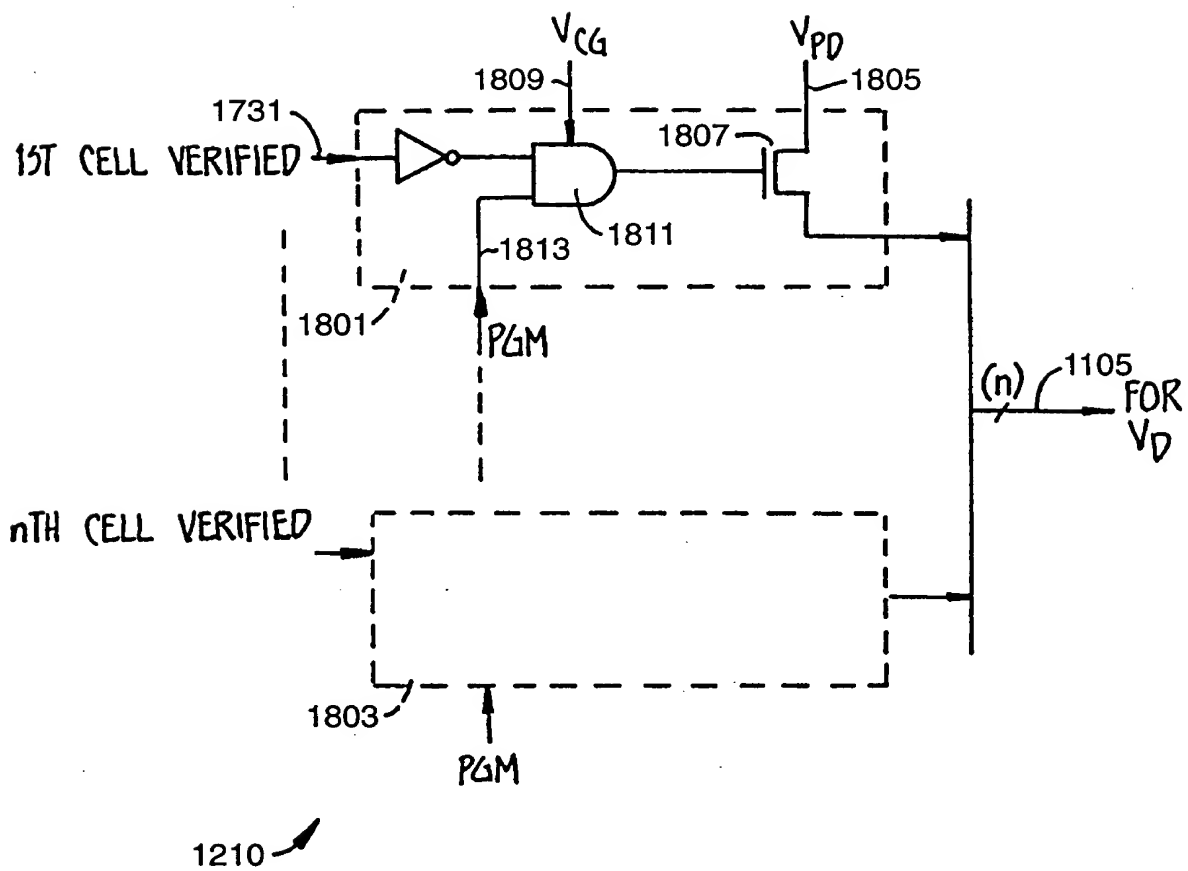


FIG. 24



**FIG. 25**

866077-1099

	SELECTED CONTROL GATE $V_{CG}$	DRAIN $V_D$	SOURCE $V_S$	ERASE GATE $V_{EG}$
READ	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
PROGRAM	$V_{PG}$	$V_{PD}$	$V_{SS}$	$V_E$
PROGRAM VERIFY	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
ERASE	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
ERASE VERIFY	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$

TABLE 1

**FIG.\_26**

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
$V_{PG}$	$V_{CC}$	12V	$V_{CC} + \delta V$	$V_{CC}$	$V_{CC} - \delta V$
$V_{CC}$	5V	5V	5V	5V	5V
$V_{PD}$	$V_{SS}$	8V	8V	$V_{SS}$	$V_{SS}$
$V_E$	$V_{SS}$	$V_{SS}$	$V_{SS}$	20V	$V_{SS}$
UNSELECTED CONTROL GATE	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$
UNSELECTED BIT LINE	$V_{REF}$	$V_{REF}$	$V_{REF}$	$V_{REF}$	$V_{REF}$

 $V_{SS} = 0V, V_{REF} = 1.5V, \delta V = 0.5V - 1V$ 

TABLE 2

**FIG.\_27**